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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/103,873	Applicant(s) NAGANO ET AL.	
	Examiner José R. Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

➢ This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102((e), f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 1-2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Wolf et al. ("Silicon Processing for the VLSI Era Volume 1: Process Technology", Lattice Press, 1986, pp. 182-194).

Regarding claims 1 and 8, Applicant acknowledges that is well known in the art to form a semiconductor device comprised of: an integrated circuit (4) on a supporting substrate (1); a capacitor (10) having a lower electrode (7), a dielectric film (8), and an upper electrode (9); a first interlayer insulating film (11) provided so as to cover the capacitor; a first interconnect (14) electrically connected to the integrated circuit (4) and

the capacitor (10) through a first contact hole (12) formed in the first interlayer insulating film (11); a second interlayer insulating film (15) formed by plasma CVD and provided so as to directly cover the first interconnect (14); a second interconnect (17) electrically connected to the first interconnect (14) through a second contact hole (16) formed in the second interlayer insulating film (15); and a passivation layer (18) provided so as to cover the second interconnect (17) (See figures 10A-10E). However, the Specification fails to disclose a second interlayer insulating film having a tensile stress. Wolf et al. teach that is well known in the art that a silicon oxide film formed by CVD process (e.g. PECVD and APCVD) would result in a film having a tensile stress of 3×10^9 dynes/cm^2 (see *stress vs. PECVD* and *stress vs. APCVD* on page 183, table 2). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Applicant's Specification to include the limitation of a silicon oxide film formed by CVD. The ordinary artisan would have been motivated to modify Applicant's Specification in the manner described above for at least the purpose of forming a silicon oxide film having a tensile stress of 3×10^9 dynes/cm^2.

Regarding claim 2, Applicant acknowledges that the dielectric film (8) is formed of either a dielectric material having a high dielectric constant or ferroelectric material (Page 2, lines 26-28).

➢ Claims 3-4, 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Wolf et al. ("Silicon Processing for the VLSI Era Volume 1: Process Technology", Lattice Press, 1986, pp. 182-194) and further in view of Yoshizumi et al. (US Patent No. 5,444,012).

Regarding claim 3, the Specification, as stated supra, essentially discloses the claimed invention but fails to disclose a second interconnect on the second interlayer insulating film provided so as to cover at least a part of the capacitor. Yoshizumi et al. teach that it is well known in the art to form a second interconnect (DL_1, DL_2) on selective portions of an insulating film (35) so as to cover at least a part of the capacitors (C_1, C_2) (Figure 24). Yoshizumi et al. provide motivation to use such a layer in that it provides a connection to the first interconnect (33) (column 21, lines 13-15). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include providing a second interconnect on the second interlayer insulating film so as to cover at least a part of the capacitor as taught by Yoshizumi et al. since such modification would result in a connection between the first and second interconnect, as described in column 21, lines 13-15 of Yoshizumi et al.

Regarding claim 4, the Specification does not disclose a passivation layer that is formed from a laminate including a silicon oxide film and a silicon nitride film. Yoshizumi et al. teach that it is well known in the art to form a passivation layer from a laminate including a silicon oxide film (37a, 37b) and a silicon nitride film (37c) (Figure 28). Yoshizumi et al. provide motivation to use such a layer in that there is no increase in the number of photomasks and the number of steps in etching (column 23, lines 57-61). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include providing a passivation layer from a laminate including a silicon oxide film and a silicon

nitride film as taught by Yoshizumi et al. since such modification would result in a decrease of the number of photomasks and the number of steps in, as described in column 23, lines 57-61 of Yoshizumi et al.

Regarding claims 6 and 10, the Specification does not disclose that the first and second interconnect layers are formed from a laminate including aluminum and titanium tungsten. Yoshizumi et al. teach that it is well known in the art to use a three-layer film formed by successive lamination of TiW film, aluminum alloy film, and TiW as the wiring material (column 20, lines 54-56). Yoshizumi et al. provide motivation to use such material in that the wiring line can be prevented from being broken by electromigration (column 21, lines 5-7). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification to include a laminate of TiW film, aluminum alloy film, and TiW as the wiring material as taught by Yoshizumi et al. since such modification would result in a wiring line having no cracks, as described in column 21, lines 5-7 of Yoshizumi et al.

➢ Claims 5, 7, 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification in view of Wolf et al. ("Silicon Processing for the VLSI Era Volume 1: Process Technology", Lattice Press, 1986, pp. 182-194) and further in view of Matsuura et al. (US Patent No. 5,132,774).

Regarding claims 5 and 28, the Specification, as stated supra, essentially discloses the claimed invention but fails to show a hydrogen supplying layer. Matsuura et al. teach forming a hydrogen supplying layer (i.e. silicon nitride) (13) (See Figure 5B). Matsuura et al. provide motivation to use such a layer in that the stress of the interlayer

insulating film (14) is relaxed (column 7, lines 3-6 and 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant to include a hydrogen supplying layer as taught by Matsuura et al. since such modification would result in a interlayer insulating film having no stress, as described in column 7, lines 3-6 and 7-10 of Matsuura et al. Furthermore, Official Notice is taken with respect to the limitation of "said hydrogen supplying layer having a sufficient amount of hydrogen" since it is well known in the art that silicon nitride is formed by using silane gas (SiH_4) and ammonia (NH_3), which have "a sufficient amount of hydrogen" (see for example Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology", page 194, table 4).

Regarding claim 7 and 9, the Specification does not teach a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} is 800 cm^{-1} or less and a thickness of 0.3 μm to 1 μm. Regarding claim 7, Matsuura et al. teach a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} (Figure 3B). Regarding claim 9, Matsuura et al. teach that it is known in the art to provide an interlayer insulating film (4) having a thickness of about 5 μm (column 1, lines 30-35). Matsuura et al. provide motivation to use such a layer having a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} and a thickness of about 5 μm in that the insulation of the semiconductor device is improved by feature of an interlayer insulating film (column 3, lines 23-25). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to have modified Applicant's Specification

to include a layer having a Si-OH bond absorption coefficient of the insulating film at a wavelength corresponding to 3450 cm^{-1} and a thickness of about 5 μm as taught by Matsuura et al. since such modification would result in an interlayer insulating film having no cracks, as described in column 3, lines 23-25 of Matsuura et al.

Response to Arguments

➢ Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

➢ Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 8:00 - 5:00 Monday through Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
August 7, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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